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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): FIS920040002US1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 8-6-07

Signature Kelly Nowak

Typed or printed name Kelly Nowak

| Application Number | Filed |
|---|---|
| 10/711,501 | September 22, 2004 |

First Named Inventor: Mukta G. Farooq et al.

| Art Unit | Examiner |
|---|---|
| 1725 | Michael Aboagye |

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [XX] attorney or agent of record. Registration number 47,898
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Kelly Nowak
Signature

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Typed or printed name

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Telephone number

8-6-07
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

DOCKET: FIS920040002US1 PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| INVENTOR: | Mukta G. Farooq et al. | EXAMINER : | Michael Aboagye |
| SERIAL NO.: | 10/711,501 | ART UNIT: | 1725 |
| FILING DATE: | September 22, 2004 | DATE: | August 6, 2007 |
| FOR: | SOLDER INTERCONNECTION ARRAY WITH OPTIMAL MECHANICAL INTEGRITY | | |

## REASONS FOR PRE-APPEAL REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Name: Kelly Nowak Date: August 6, 2007
Signature: Kelly Nowak

Dear Sir:

Applicants are submitting these remarks to accompany their Notice of Appeal and Pre-Appeal Brief Request for Review.

Applicants submit that claims 1-10 and 13-22 are pending.

No new matter has been added.

**Claim Rejections - 35 USC § 103**

*Claims 1-5, 7-10, 13, 14, 19 and 20*

Claims 1-5, 7-10, 13, 14, 19 and 20 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. US Patent No. 6,333,563 (hereinafter "Jackson") in view of Peterson US Patent No. 5,011,870 (hereinafter "Peterson").

Claim 6 stands finally rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 5, and further in view of Cui US Patent No. 6,274,650 (hereinafter "Cui").

Claims 14-18 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 5, and further in view of Kumamoto et al. US Patent No. 6,632,704 (hereinafter "Kumamoto").

Claims 21 and 22 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson et al. in view of Peterson as applied to claim 1 and 19, and further in view of Morganelli et al. US Patent No. 7,047,633 (hereinafter "Morganelli").

Applicants respectfully traverse these rejections and request review on the grounds that the Examiner's citation of the prior art lacks essential elements to establish *prima facie* rejections for obviousness.

It is submitted that the independent claims, to wit, claims 1, 5 and 19, and the claims dependent thereon, are all directed toward methods for assembling an electronic module and an electronic module assembled by such methods. In accordance with the invention, a chip is attached to a substrate using a first solder interconnection array and a board (an organic board) is attached to the substrate using a second solder interconnection array such that a space is defined between the board and substrate. The second solder interconnection array resides entirely within this space, which has a gap height ranging from about 300 microns to about 900 microns. An underfill material is provided within the space prior to applying compressive forces to the electronic module. This underfill material has a filler material with a particle size ranging from about 32 microns to about 300 microns that is present in an amount ranging from about 60 to 64 weight percent.

An essential feature of applicants' invention is that the underfill material directly contacts both the board and substrate to maintain the space therebetween and optimize the integrity of the second solder interconnection array during application of compressive forces. In accordance with claim 5, this underfil material may be deposited at discrete locations within the space so that the underfill material contacts both the board and substrate, as well as selected solder joints, for partially encapsulating the second solder interconnection array at these discrete locations. The underfill is then cured to form a rigid matrix within the space to maintain and enhance integrity of the second solder interconnection array.

In the invention, where the space has a gap height from about 300 microns to about 900 microns, the underfill material (in its uncured state) may be a polymeric material having a filler material present in an amount ranging from about 60% to about 64% by weight per solution, and having a particle size ranging from about 32 to about 300 microns in diameter.

With respect to the Jackson reference, the Examiner acknowledges that Jackson does not teach providing an underfill material in a space between a circuit board and a substrate.

To overcome this deficiency, the Examiner cites Peterson stating that it discloses an underfill or an encapsulate material used in the process of mounting a solid state electronic device to a circuit board to improve the thermal conductive between the components of the assembly; wherein the underfill material is composed of an organic binder and a filler material having particle size ranging from 20-100 microns and the filler constituting about 40-85 percent of the total weight of the underfill, wherein a higher thermal conductivity is achieve and thereby avoiding the problems associated with CTE mismatch ( Peterson, column 1, lines 13-30, column 2, line 42- column 3, lines 25, column 3, lines 35-40, and column 4, lines 1-34)." It is the Examiner's position that it would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to have modified the method of Jackson et al. with depositing a filler material between the substrate and the board, with a filler material composition as taught by Peterson in order to achieve a higher thermal conductivity is achieve and thereby avoiding the problems associated with CTE mismatch (Peterson, column 1, lines 13-30, column 2, line 42- column 3, lines 25, column 3, lines 35-40, and column 4, lines 1-34).

Applicants disagree. It is submitted that Peterson is limited to organosiloxanes for use as coatings and encapsulates of electronic devices and the circuit boards on which these devices are often mounted. (Col. 1, ll. 13-18.) That is, the circuit board itself is coated or encapsulated. In the advisory action dated July 6, 2007, the Examiner states that Peterson teaches a no-flow underfill process in which an encapsulate is applied to a board before the electronic device is mounted, and that the encapsulate material, per location in the assembly, is between the board and the electronic device mounted on the board. The Examiner further states that the pending claims, given their broadest reasonable interpretation, are met by Peterson. Applicants disagree and submit that like Jackson, Peterson does not disclose, contemplate or suggest that an underfill material directly contacts both a board and a substrate to maintain the space therebetween and optimize the integrity of a second solder

interconnection array during application of compressive forces, as is currently claimed. Again, Peterson is limited to coatings and encapsulates. (Col. 1, ll. 13-18.) The Examples of Peterson also show that the compositions disclosed therein are to be applied as smooth, coherent coatings to protect the electronic devices (*see*, col. 5, l. 54 to col. 7, l. 30) from contact with moisture, corrosive materials and other impurities present in the environment in which these devices operate (col. 1, ll. 18-28).

Further, the compositions of the present invention are different from the composition of Peterson. Peterson discloses a composition of a polyorganosiloxane and a thermally conductive filler, whereby the thermally conductive filler is a mixture that constitutes from 40% to 85% of the total weight of the composition. (Col. 2, l. 58 to col. 3, l. 2.) The thermally conductive filler has aluminum nitride present in the thermally conductive filler mixture from 20 to 60 weight percent (col. 3, ll. 64-66) and having an average particle size no larger than one micron and a second filler having an average particle size of from 10 to 100 microns. (Col. 2, l. 58 to col. 3, l. 2.) That is, of the weight percent of the overall composition, the thermally conductive filler is present in the composition from about 20-60 weight percent. Applicants submit that this is a difference in kind, and not of degree.

The Examples and Table 2 of Peterson also show that its thermal conductivity is maximized when the weight ratio of the second filler (silicon metal) to the first filler (aluminum nitride) is 1:1 and 4:1. As such, Peterson's composition of 80 weight percent of the filler mixture, which in the 4:1 ratio comprises 64 weight percent Si metal to 16 weight percent AlN, does not equate to Peterson's composition of polyorganosiloxane and a thermally conductive filler (which constitutes 40% to 85% of the total weight of the composition) having a filler with a particle size ranging from about 32 microns to about 300 microns present in an amount ranging from about 60 to 64 weight percent of the composition, as is currently claimed. (Col. 7, l. 30 to col. 8, l. 16.)

In the Advisory Action dated July 6, 2007, the Examiner states that applicants argument regarding a second filler is not pertinent to the claimed invention, however, applicants point out that the second filler of Peterson is only discussed to show that Peterson's composition of a polyorganosiloxane and a thermally conductive filler is different from that of applicants' claimed underfill material.

As for claim 6, applicants submit that claim 5 is not obvious over Jackson et al. in view of Peterson since neither Jackson et al. nor Peterson, alone or in combination, disclose,

contemplate or suggest the limitations as recited in claim 5. Cui does not overcome the deficiencies of Jackson or Peterson, either alone or in combination.

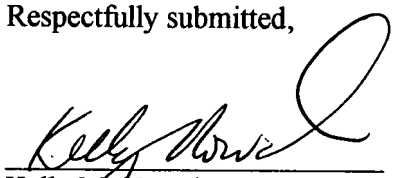
As for claims 14-18, applicants submit that claim 5 is not obvious over Jackson et al. in view of Peterson since neither Jackson et al. nor Peterson, alone or in combination, disclose, contemplate or suggest the limitations as recited in claim 5. Kumamoto does not overcome the deficiencies of Jackson or Peterson, either alone or in combination.

Applicants continue to submit that the suggestion to make the claimed structure, carry out the claimed process and the reasonable expectation of success there-from must be founded in the prior art, not in Applicant's disclosure. *In re Vaech* (CAFC 1991) 20 USPQ2d 1438. The cited reference, and not in retrospect, must suggest doing what Applicants have done. *In re Skoll* (CCPA 1975) 187 USPQ 481. Applicants submit that the cited references, alone or in combination, do not suggest doing what applicants have done, such that applicants' invention would only be found based on applicants' own disclosure, which of course is improper as a hindsight reconstruction of applicants' invention. *Id., W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983) (Hindsight based on reading of the patent in issue may not be used to aid in determining obviousness). Likewise, hindsight and the level of ordinary skill in the art may not be used to supply a component missing from the cited references. *Al-Site Corp. v. VSI International, Inc.*, 174 F.3d 1308, 1324, 50 USPQ2d 1161, 1171 (Fed. Cir. 1999).

It is for these reasons that applicants submit that the Examiner has not established a *prima facie* case of obviousness over Jackson et al., Peterson, Cui, Kumamoto, or Morganelli, alone or in any proper combination thereof.

Applicants submit that the application is in a condition where allowance of the entire case is proper. Reconsideration and issuance of a notice of allowance are respectfully solicited.

Respectfully submitted,



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